AN13468

i.MX RT600 Power Management

Rev. 1 — 07 April 2022 Application Note

Contents

1 Introduction

This document describes the power architecture of the i.MXRT600 and shows all the internal loads of the part and how to control them. It also provides guidance on typical 25C currents based on bench measurements but is not intended to replace the data sheet.

2 Power rails and distribution

The figure below shows a high-level diagram with some of the power domains in the i.MX RT600.

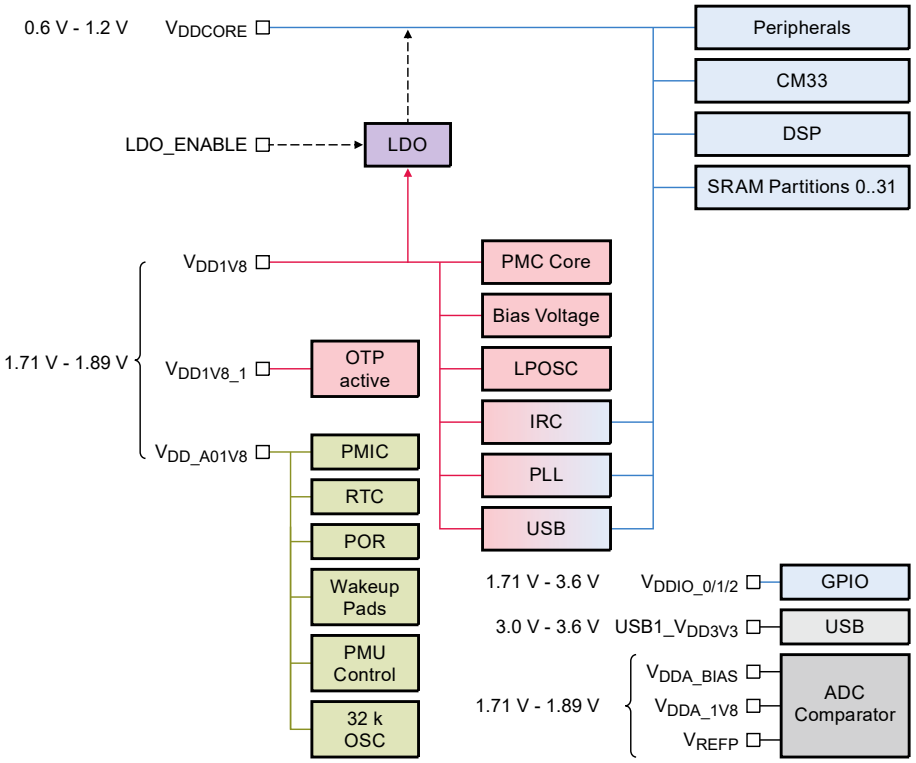

Figure 1. Power Domains

2.1 VDD_Core

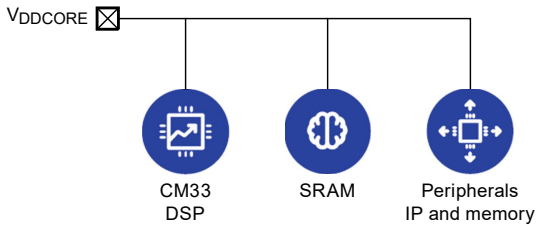

Figure 2. VDD_Core Loads

VDD_Core is an adjustable voltage from 0.7 V to 1.155 V. The minimum VDD_Core voltage level in active mode gets determined by the core frequency, as shown in Table 1. For SDK version 2.8 and before (SDK Power Library version = 0x020200): The maximum frequency for the specified VDDCORE voltage is the frequency of the main clock. This is before the CPU CLOCK Divider. The VDDCORE voltage has to be set according to the chosen main clock frequency. For SDK version 2.8.3 and after (SDK Power Library version = 0x02030): The maximum frequency for the specified VDDCORE voltage is the frequency of the clock after CPU CLOCK and DSP clock Divider.

Table 1. VDD_Core minimum voltage in Active mode

Frequency	min V_{DD_Core}
65 MHz	0.7 V
140 MHz	0.8 V
210 MHz	0.9 V
275 MHz	1.0 V
300 MHz	1.13 V

2.2 VDD1V8

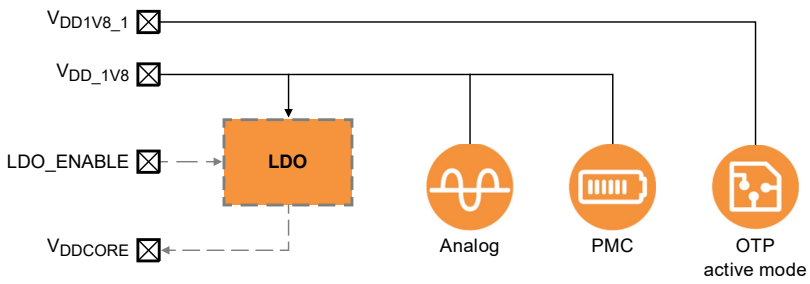

Figure 3. VDD1V8

2.2.1 VDD1V8

1.8 V voltage supply is used for on-chip analog functions other than the ADC and comparator. It is also a power supply to the Power Management Core. That includes band gap, POR, temperature sensor, core low-voltage, and high-voltage detection. In addition, it powers the Low-power oscillator, the slow, and fast IRC and the PLL.

2.2.2 VDD1V8_1

1.8 V supply voltage is used for OTP during active mode. In deep-sleep mode, this pin can be powered off to conserve additional current (~ 65 uA). VDD1V8_1 must be stable before performing any OTP-related functions.

2.2.3 VDD_AO1V8

Supply 1.8 V is used for “always on” features. It includes RTC, RESETN, LDO_ENABLE, PMIC_IRQ_N, PMIC_MODE0, and PMIC_MODE1.

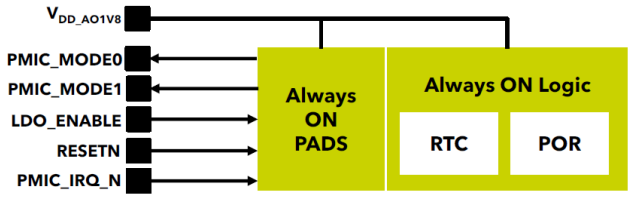

Figure 4. Always-ON Domain

2.2.4 VDDA_1V8

1.8 V analog supply voltage is used for ADC and comparator.

2.2.5 LDO_ENABLE

The LDO_ENABLE pin is used to select whether V_{DDCore} is powered using the internal LDO or an external source. When the LDO_ENALBE pin is pulled high, V_{DDCore} is supplied from the internal LDO and the LDO is powered from the V_{DD1V8}. When the LDO_ENABLE pin is pulled low, V_{DDCore} is supplied from an external source.

2.3 VDDIO

This section gives the details of VDDIO.

2.3.1 VDDIO_0/1/2

Supply voltage for GPIO pins. VDDIO_0, VDDIO_1, and VDDIO_2 may be supplied at different voltage levels as needed by the application.

2.4 VDD_BIAS

VDD_BIAS is a bias for ADC and comparator. VDD_BIAS must be equal to the highest VDDIO rail voltage used for the ADC input channel or comparator inputs.

3 Power modes

i.MXRT600 module implements five basic power modes: Active, Sleep, Deep Sleep, Deep Power-down, and Full Deep Power-down. The following sections explain the difference between power modes, using the following de-coding bullets.

↑ ON

→ Software selection ON, OFF, or Low Power

↓ OFF

3.1 Active

The device is in active mode after RESET and the default power configuration is determined by the boot values of the PDRUNCFG and PSCCTL registers.

↑ CPU, Enabled Memories, and Peripherals.

3.1.1 Active mode (dynamic) power consumption

The following sections show typical bench power data for the core and DSP domains.

3.1.2 Core domain dynamic power

Table 2. Core dynamic current

Conditions DSP OFF enhanced while (1) code executed from SRAM; Internal LDO disabled	$I_{DDVDDCore}$
CCLK = 12 MHz V_{DDCore} = 0.7 V	3.0 mA
CCLK = 48 MHz V_{DDCore} = 0.7 V	6.0 mA
CCLK = 60 MHz V_{DDCore} = 0.7 V	7.0 mA
CCLK = 80 MHz V_{DDCore} = 0.8 V	10 mA
CCLK = 110 MHz V_{DDCore} = 0.8 V	13 mA
CCLK = 144 MHz V_{DDCore} = 0.9 V	19 mA
CCLK = 180 MHz V_{DDCore} = 0.9 V	23 mA
CCLK = 204 MHz V_{DDCore} = 0.9 V	26 mA
CCLK = 240 MHz V_{DDCore} = 1.0 V	34 mA
CCLK = 270 MHz V_{DDCore} = 1.0 V	38 mA

Table continues on the next page...

Table 2. Core dynamic current (continued)

Conditions DSP OFF enhanced while (1) code executed from SRAM; Internal LDO disabled	$I_{DDVDDCore}$
CCLK = 300 MHz V_{DDCore} = 1.13 V	50 mA

3.1.3 DSP domain dynamic power

- The DSP sits in its own power island that can be turned on and off.
- The table shows consumption running an FFT.
  - Leakage current is what is present when the DSP is switched on.
  - Dynamic current reflects operating frequency.
- For example, consumption at 0.8 V and 100 MHz:

  $6.79mA + 10uA = 6.8mA\ or\ 5.44mW$

Table 3. DSP dynamic current

Conditions CM33 WFI FFT code executed from SRAM partition 12; Internal LDO disabled	$I_{DDVDDCore}$
CCLK = 12 MHz V_{DDCore} = 0.7 V	4.6 mA
CCLK = 48 MHz V_{DDCore} = 0.7 V	11 mA
CCLK = 60 MHz V_{DDCore} = 0.7 V	14 mA
CCLK = 80 MHz V_{DDCore} = 0.8 V	20 mA
CCLK = 110 MHz V_{DDCore} = 0.8 V	27 mA
CCLK = 144 MHz V_{DDCore} = 0.8 V	34 mA
CCLK = 180 MHz	42 mA

Table continues on the next page...

Table 3. DSP dynamic current (continued)

Conditions CM33 WFI FFT code executed from SRAM partition 12; Internal LDO disabled	$I_{DDVDDCore}$
V_{DDCore} = 0.8 V	
CCLK = 204 MHz V_{DDCore} = 0.8 V	47 mA
CCLK = 240 MHz V_{DDCore} = 0.9 V	63 mA
CCLK = 270 MHz V_{DDCore} = 0.9 V	71 mA
CCLK = 300 MHz V_{DDCore} = 0.9 V	78 mA
CCLK = 400 MHz V_{DDCore} = 1.0 V	117 mA
CCLK = 600 MHz V_{DDCore} = 1.13 V	207 mA

3.2 Sleep

Sleep mode occurs when an interrupt is enabled or when a reset occurs. The device then returns to its original power configuration defined by the contents of the `PDRUNCFG` and `PSCCTL` registers. If a reset occurs, it enters the default configuration in Active mode.

↓ Stop the clock to the CPU (system clock).

↓ Suspend instruction execution until RESET or an interrupt occurs.

→ You can block the Peripherals and continue the operation.

→ Peripherals can generate interrupts to resume execution.

→ SRAM that was not shut down maintain their content.

↑ CPU state and registers and peripheral registers are maintained.

↑ Pins logic levels remain static.

3.2.1 Sleep mode power consumption

Table 4. Core power consumption in Sleep mode

Conditions DSP OFF enhanced while (1) code executed from SRAM; Internal LDO disabled	$I_{DDVDDCore}$
CCLK = 12 MHz V_{DDCore} = 0.7 V	3.0 mA
CCLK = 48 MHz V_{DDCore} = 0.7 V	4.0 mA
CCLK = 250 MHz V_{DDCore} = 1.0 V	20.3 mA

3.3 Deep Sleep

The Deep Sleep mode is configurable and can potentially turn off nearly all on-chip power consumption other than the on-chip power supply, with the cost of a longer wake-up time.

↓ Stop clock to the CPU (system clock).

↓ Power consumed by analog peripherals, dynamic power used by the processor.

→ Peripherals, if not configured, receive no internal clocks.

→ GPIO Pin Interrupts, and selected peripherals can be left running.

→ SRAM that was not shut down maintain their content.

→ Analog blocks are powered down by default but can be software-configured.

↑ CPU state and registers and peripheral registers are maintained.

↑ Pins logic levels remain static.

Before going into Deep Sleep, ensure that:

1. Active mode VDDCORE ≥ LVDCORECTRL.LVDCORELVL + 20 mV.
2. Deep Sleep mode VDDCORE < LVDCORECTRL.LVDCORELVL.

If it is not done, your application hangs and never fully wakes up. It is because when using an external PMIC, on initial power-up and on wake-up from Deep Sleep, the PMC logic uses the LVD status to determine when VDDCORE is high enough to allow the MCU to operate. There is no other handshake with the PMIC to indicate to the PMC that VDDCORE is OK for operation. For example, when the LVD trip is set to the minimum (0.72 V) and the application is using an external PMIC, the VDDCORE must drop below 0.72 V in the Deep Sleep mode and rise above 0.74 V when waking up (it is 0.72 V + 20 mV hysteresis).

3.3.1 Deep Sleep power consumption

- Current Consumption
  - Core leakage + memory leakage
    - With 5 MBytes, retained leakage on current samples is between 80-90uA @ 0.6 V.
    - With 32 KB, retained leakage on current samples is between 40-50uA @ 0.6 V.
    - Total leakage power is between 48-54uW

- Memories are 6uW/Mbyte

— Pad leakage

- Pads can be power switched to turn off leakage

Table 5. Voltage domain dynamic current

Pad segment	Conditions All power supplies = 1.8 V, except USB1_VDD3V3 = 3.3 V	Current consumption
I_{VDD1V8}	SRAM (128 KB) powered, Internal LDO enabled. Array On, Periphery Off	109 µA
I_{VDD1V8_1}	SRAM (128 KB) powered, Internal LDO enabled. Array On, Periphery Off	65 uA
$I_{VDDCORE}$	SRAM (32 KB) powered, Internal LDO disabled. Array On, Periphery Off	75 uA
$I_{VDDCORE}$	SRAM (128 KB) powered, Internal LDO disabled. Array On, Periphery Off	77 µA
$I_{VDDCORE}$	SRAM (4.5 MB) powered, Internal LDO disabled. Array On, Periphery Off	190 mA
I_{VDD_AO1V8}	SRAM (128 KB) powered, Internal LDO enabled. Array On, Periphery Off	0.6 µA
I_{VDDIO_0}	SRAM (128 KB) powered, Internal LDO enabled. Array On, Periphery Off	7.0 uA
I_{VDDIO_1}	SRAM (128 KB) powered, Internal LDO enabled. Array On, Periphery Off	0.9 uA
I_{VDDIO_2}	SRAM (128 KB) powered, Internal LDO enabled. Array On, Periphery Off	6.4 uA
I_{VDDA_1V8}	SRAM (128 KB) powered, Internal LDO enabled. Array On, Periphery Off	0.1 uA
I_{VDDA_BIAS}	SRAM (128 KB) powered,	0.1 uA

Table continues on the next page...

Table 5. Voltage domain dynamic current (continued)

Pad segment	Conditions All power supplies = 1.8 V, except USB1_VDD3V3 = 3.3 V	Current consumption
	Internal LDO enabled. Array On, Periphery Off	
I_{VREFP}	SRAM (128 KB) powered, Internal LDO enabled. Array On, Periphery Off	0.1 uA
I_{USB1_VDD3V3}	SRAM (128 KB) powered, Internal LDO enabled. Array On, Periphery Off	0.1 µA

3.4 Deep Power-down

Wake-up from Deep Power-Down is done through RESET or RTC.

↓ Shut OFF the entire chip clock and power.

↓ SRAM and register content are not retained.

↓ All functional pins are tri-stated as long as supplied externally.

↑ External supplies are powered ON.

↑ V_{DD_AO1V8} is ON, then RTC is ON.

3.4.1 Optimizing power in the Deep Power-down mode

The Deep Power-Down mode has no configuration options. All clocks, the core, and all peripherals are powered down. Only the RTC is powered, as long as power is supplied to the VDD_AO1V8 pin.

3.4.2 Deep Power-down power consumption

- VDDCORE <1 uA
- Ports with high-speed pads must be turned off externally.
  - VDDIO_0 – VDDIO_2 & VDDIO_4
  - If ports are off, the pads are fail-safe.
- VDDIO_3 does not have high-speed pads.
  - Leakage current is less that 50 nA.
- Total deep power down current is <1.5 uA if VDDIO_1, VDDIO_2, and VDDIO_4 are load switched.

3.5 Full Deep Power-down

External power must be restored prior to wake-up. Wake-up from full Deep Power-down is done through RESET or RTC.

↓ Shut OFF the entire chip clock and power.

↓ SRAM and register content are not retained.

↓ All functional pins are tri-stated as long as supplied externally.

↓ External supplies are powered OFF.

↑ V_{DD_AO1V8} is ON then RTC is ON.

3.5.1 Full Deep Power-down power consumption

Table 6. Core power consumption in full Deep Power-down

Pad segment	Conditions All power supplies = 1.8 V, except USB1_VDD3V3 = 3.3 V	Current consumption
I_{VDD_AO1V8}	LDO disabled. RTC Off	0.6 uA

3.6 Power mode transitions

Transitions from active mode to various low-power modes are initiated by software and wakeups are triggered by hardware events (resets or interrupts previously configured by software). Entering Deep Sleep or Deep Power-down modes is initiated by first configuring `PDSLEEPCFG` to select off/on/low power mode for various blocks and then executing the `ARM WFI` command in the M33 core. Wake-up from any sleep or Power-down mode is triggered by an active wake-up source or reset or POR. It is summarized in the figure below:

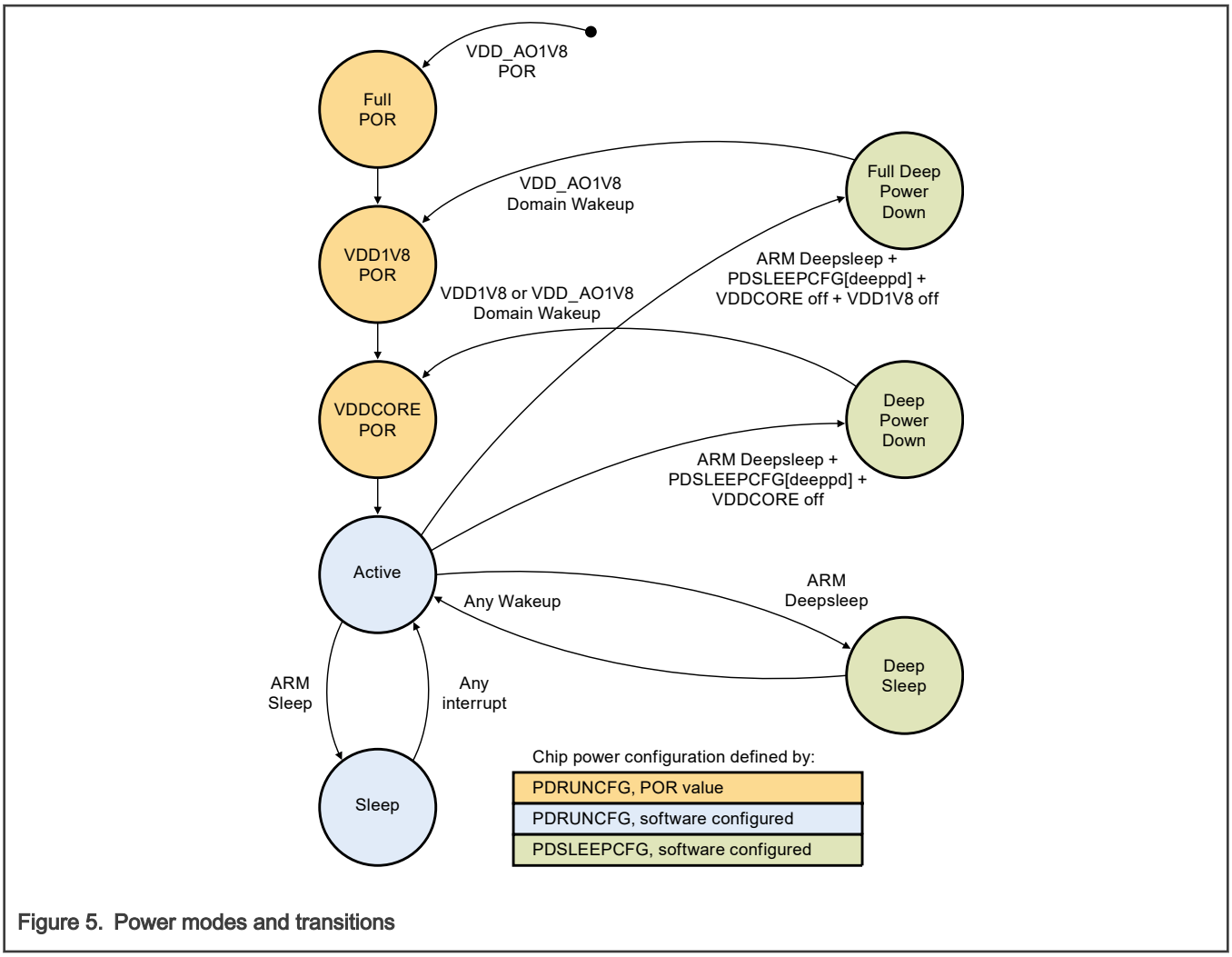

Figure 5. Power modes and transitions

4 Pad Group currents

RT600 has 3 pad groups, VDDIO_0-VDDIO_2. Each pad group has a separate rail so they can all be powered by different voltage levels ranging from 1.71 V to 3.6 V.

4.1 Pad Group GPIOs

The following table shows GPIOs belonging to the specific pad group.

Table 7. GPIO pins associated to the pad group

Pin	GPIO Pins
VDDIO_0	PIO0_0 to PIO0_13 PIO1_11 to PIO1_29 PIO2_12 to PIO2_23 PIO3_25 to PIO3_31 PIO4_0 to PIO4_10 PIO7_24 to PIO7_31
VDDIO_1	PIO0_14 to PIO0_31 PIO1_0 to PIO1_10 PIO2_24 to PIO2_31 PIO3_0 to PIO3_24 PMIC_I2C_SCL PMIC_I2C_SDA
VDDIO_2	PIO1_30 to PIO1_31 PIO2_0 to PIO2_11

Depending on what voltage is applied to the VDDIO_x rail, the appropriate range setting must be configured in the PADVRANGE register shown in Table 8

Table 8. PADVRANGE – PMC GPIO VDDIO Range Selection Control

VDDIO_xRANGE	Description	Reset Value
00	Voltage from 1.71 V to 3.6 V (wide voltage range). Consumes static current to detect the VDDIO0 level. It is recommended to change this value to 01 to reduce power consumption.	0x0
01	Voltage from 1.71 V to 1.98 V (low-voltage range), VDDIO detector off.	
10	Voltage from 3.0 V to 3.6 V (high-voltage range), VDDIO detector off.	
11	Reserved	-

5 Clock gating

RT600 supports the ability to clock-gate various AHB peripherals and SRAMs. It can be accomplished in two ways: automatic and manual clock gating.

5.1 Automatic clock gating

Automatic clock gating turns off the bus clock to the related function if it is not accessed for 16 clocks. A subsequent access incurs a one clock delay for the clock gate to be turned on.

The following registers automatically control clock gating:

Table 9. Control gating peripherals

Auto clock gating register	Selected functions
SYSCTL0_AUTOCLKGATEOVERRIDE0	AHB2APB0 AHB2APB1 CRC_ENGINE CASPER DMAC0 DMAC1
SYSCTL0_AUTOCLKGATEOVERRIDE1	SRAMIF0 - SRAMIF29
SYSCTL0_CLKGATEOVERRIDE0	SDIO_0 SDIO_1 USBHSPHY ADC MU ACMP PMC

While the primary purpose of these registers is to block access to a particular commander, an alternate effect is to prevent the associated clock from being propagated. It can result in a significant reduction in power in the case where a partition is not being used.

6 Code locality

The use of the different SRAM partitions results in different current consumption. It is due to the physical location of the various partitions on the chip. For example, the following list outlines the current draw from lowest to highest SRAM partition running an advance-while 1, Typical, 25C, NBB, 198 MHz (FRO), all memories ON (only one partition clocked):

Table 10. Current draw from lowest to highest SRAM partition

Partition #	IVDDCORE	Size (KB)
2	26.6	32

Table continues on the next page...

Table 10. Current draw from lowest to highest SRAM partition (continued)

Partition #	IVDDCORE	Size (KB)
3	27.1	32
4	27.6	32
5	27.5	32
6	27.1	32
7	26.9	32
8	30.0	64
9	28.8	64
10	30.7	64
11	30.1	64
12	36.2	128
13	34.9	128
14	34.3	128
15	33.4	128
16	26.6	256
17	25.8	256
18	26.7	256
19	25.4	256
20	27.5	256
21	27.0	256
22	29.1	256
23	27.4	256
24	27.0	256
25	27.9	256
26	27.8	256
27	27.1	256

Table continues on the next page...

Table 10. Current draw from lowest to highest SRAM partition (continued)

Partition #	IVDDCORE	Size (KB)
28	26.7	256
29	27.5	256

7 Body bias

RT600 offers three different body bias modes for greater power optimization flexibility: No Body Bias (NBB), Reverse Body Bias (RBB), and Forward Body Bias (FBB). The table below describes when to use each mode and how to enable them.

Table 11. Body bias modes

Mode	When to use	Bits to consider[2]	How to enable using Power Library
NBB	Very low frequencies (for example, <60 MHz @ 0.7 V)	PDRUNCFGO [RBB_PD] = 1 PDRUNCFGO [FBB_PD] = 1 PDRUNCFGO [MAINCLK_SHUTOFF] = 1	Power_EnterNBB
RBB	Only in Deep Sleep mode	PDRUNCFGO [RBB_PD] = 0 PDRUNCFGO [FBB_PD] = 1 PDRUNCFGO [MAINCLK_SHUTOFF] = 1	Power_EnterRBB
FBB[1]	All other use cases	PDRUNCFGO [RBB_PD] = 1 PDRUNCFGO [FBB_PD] = 0 PDRUNCFGO [MAINCLK_SHUTOFF] = 1	Power_EnterFBB

1. Default mode

2. There is a specific process that must be followed when switching between body bias modes, which is why we recommend only using the power library API to switch modes.

If the OTP is not powered down in `PDRUNCFG/PDSLEEPCFG`, the default setting leaves it in Standby mode, which consumes about 600 uA on `VDDCORE`, and 2.1 mA on `vdd_fuse18` in typical conditions.

8 Fuse block current consumption

The fuse block is used for security, trimming, and user configuration options. The fuse block also referred to as the OTP block has two distinct parts as shown in the figure below: one is where the fuse cells reside and the other is the control and access logic for the fuse bits. The fuse cell part contains analog circuits for programming and reading the cells. The RT600 design added a switch to turn off the analog part of the fuse block.

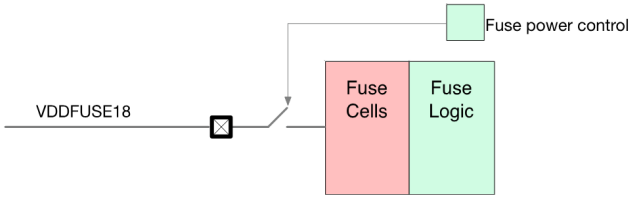

Figure 6. Fuse block

9 RTC current consumption

Independent power island.

Two power pins are as shown in the figure below.

- VDD_AO18 supplies crystal and logic:
  - Logic consumption: 600-700nA.
  - Crystal: 200 nA.
  - Total RTC current 800-900nA.
- VDDEA0 supplies the pads:
  - Leakage current is less than 50 nA.

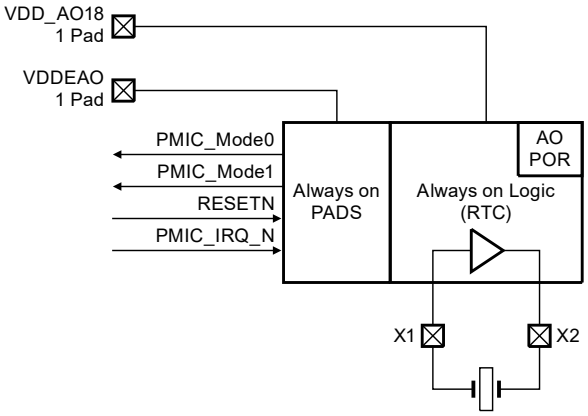

Figure 7. RTC pads

10 Optimization techniques

This section is dedicated to optimization techniques in different modes.

10.1 Optimizing power in Active mode

To minimize power consumption in Active mode, do the following:

1. Power down unused blocks via the PDRUNCFG0/1/2/3 registers. Power Down (PD) bits and other power controls include:
   - PD bits for all Analog blocks (incl oscillators, PHYs, and so on)
   - SRAM array and periphery power switches

- Disable array and periphery of unused SRAM partitions.

- Set the correct PMIC mode pins (depending on how the PMIC was configured) if using an external PMIC.
  - The power library uses mode 00 for Active mode, configure the PMIC accordingly.
- VDDCORE high-power / low-power mode control
- Set the correct body bias mode according to Table 7.
  - These bits are automatically configured by the power library according to the power mode, try not to modify these bits.
  - Refer to the Body bias section for more information.
- PLL enables (analog and digital)
- HS pad controls
- DSP, OTP, and ROM power-off switches.
  - When the OTP bit is powered off, the OTPSWREN bit in the PMC CTRL register must also be set. If the RT600 power library is used, it is done automatically.
- Software must not set the MAINCLK_SHUTOFF bit in PDRUNCFG0; otherwise, the clocks cannot be turned back on because software cannot run without clocks and the wake-up sources are not enabled because the chip is still in Active mode.
- When the chip is running and the VDDCORE regulator is in HP mode (VDDCOREREG_LP=0), putting the LVD and PORs into LP mode (PORCORE_LP=1 and LVDCORE_LP=1) only saves about 14 uA.

2. Disable individual bus clocks for peripherals and memories via the PSCCTL0/1/2 registers.
   - These bus clocks are typically used when writing to or reading from each peripheral's register space. Clocks must be turned off when the peripheral is not in use. Some of them must be turned off after the peripheral is initialized (for example, IOCON)
3. Set the power mode for the Xtal Oscillator. It is recommended that the High-gain mode is used in high-noise environments or with jitter sensitive applications; otherwise, use low-power mode.
4. If the 32 kHz oscillator is not being used, make sure to disable it by clearing bit 0 (ENA32KHZ) in OSC32KHZCTL0 and setting bit 8 (RTC_OSC_PD) in RTC CTRL.
   - Both ENA32KHZ and RTC_OSC_PD must be configured to enable/disable the 32 kHz Oscillator.
5. Disable any unused PFD outputs via the SYSPLLOPFD register.
   - Bits [5:0], [13:8], [21:16] and [29:24] establish the PFD output frequencies for PFD0,1,2,3 respectively (For a given VCO base frequency). Bits 7, 15, 23 and 31 gate off the corresponding PFD outputs entirely.
6. Select input 7 for unused peripherals for all the various functional clock muxes (*xxx*FCLKSEL Registers) in CLKCTL.

- Selecting input 7 shuts off the clock tree entirely to that peripheral.

10.2 Optimizing power in Sleep mode

Refer to the Optimizing power in Active mode section.

10.3 Optimizing power in Deep Sleep mode

Power consumption in Deep Sleep mode is primarily determined by enabled analog wake-up sources. Serial peripherals and pin interrupts configured to wake up the contribute to the power consumption only to the extent that they are clocked by external sources. All wake-up events (other than reset) must be enabled in the NVIC. In addition, any related analog block (for example, the RTC oscillator or the watchdog oscillator) must be explicitly enabled in the call to the power API function.

1. Power down unused blocks in Deep Sleep via the PDSLEEPCFG0/1/2/3 registers. Power Down (PD) bits and other power controls include:

- Disable all SRAM periphery (PDSLEEPCFG3) and only keep the SRAM array enabled (PDSLEEPCFG2) for the SRAM partitions you wish to retain.
- Set the MAINCLK_SHUTOFF bit in PDSLEEPCFG0 if main_clk is left enabled in Deep Sleep mode.
  - For faster wake-up time, the FRO can be left enabled in Deep Sleep mode. In that case, there is a MAINCLK_SHUTOFF bit in the PDRUNCFG0. With that set, the main_clk is gated off when the MCU enters Deep Sleep mode, and most of the FRO clock tree is not active.
- Set the correct PMIC mode pins (depending on how the PMIC was configured) if using external PMIC.
  - The power library uses mode 01 for Deep Sleep mode, configure PMIC accordingly.
- VDDCORE LP/HP control
  - The VDDCORE regulator must be put into LP mode during Deep Sleep mode when there is little to no activity in the chip.
- Set the Body Bias mode to RBB.
  - These bits are automatically configured by POWER_EnterDeepSleep API.
  - Refer to the Body bias section for more information.
- PLL enables (analog and digital)
- HS pad controls
- DSP, OTP, and ROM power-off switches.
  - When the OTP bit is powered off, the OTPSWREN bit in the PMC CTRL register must also be set. If the RT600 power library is used, it is done automatically.
- In Deep Sleep mode, with all the PMU in LP mode it makes sense to put the monitors into LP mode (PORCORE_LP and LVDCORE_LP).

2. See items 2-7 in the Optimizing power in Active mode section.

10.4 Optimizing power in Full Deep Power-down mode

Full Deep Power-down mode has no configuration options.

11 References

1. i.MX RT6xx User manual (document:UM11159)

2. i.MX RT600 Rev B0 Data Sheet

3. AN12094-Power consumption and measurement (document:AN12094)

4. AN12844-Power consumption and measurement of i.MX RT6xx DSP (document:AN12844)

12 Revision history

Table 12. Revision history

Revision number	Date	Substantive changes
1	07 April 2022	• Updated VDD_Core • Updated Table 10
0	14 December 2021	Initial release

Legal information

Definitions

Draft — A draft status on a document indicates that the content is still under internal review and subject to formal approval, which may result in modifications or additions. NXP Semiconductors does not give any representations or warranties as to the accuracy or completeness of information included in a draft version of a document and shall have no liability for the consequences of use of such information.

Disclaimers

Limited warranty and liability — Information in this document is believed to be accurate and reliable. However, NXP Semiconductors does not give any representations or warranties, expressed or implied, as to the accuracy or completeness of such information and shall have no liability for the consequences of use of such information. NXP Semiconductors takes no responsibility for the content in this document if provided by an information source outside of NXP Semiconductors.

In no event shall NXP Semiconductors be liable for any indirect, incidental, punitive, special or consequential damages (including - without limitation - lost profits, lost savings, business interruption, costs related to the removal or replacement of any products or rework charges) whether or not such damages are based on tort (including negligence), warranty, breach of contract or any other legal theory.

Notwithstanding any damages that customer might incur for any reason whatsoever, NXP Semiconductors' aggregate and cumulative liability towards customer for the products described herein shall be limited in accordance with the Terms and conditions of commercial sale of NXP Semiconductors.

Right to make changes — NXP Semiconductors reserves the right to make changes to information published in this document, including without limitation specifications and product descriptions, at any time and without notice. This document supersedes and replaces all information supplied prior to the publication hereof.

Suitability for use — NXP Semiconductors products are not designed, authorized or warranted to be suitable for use in life support, life-critical or safety-critical systems or equipment, nor in applications where failure or malfunction of an NXP Semiconductors product can reasonably be expected to result in personal injury, death or severe property or environmental damage. NXP Semiconductors and its suppliers accept no liability for inclusion and/or use of NXP Semiconductors products in such equipment or applications and therefore such inclusion and/or use is at the customer's own risk.

Applications — Applications that are described herein for any of these products are for illustrative purposes only. NXP Semiconductors makes no representation or warranty that such applications will be suitable for the specified use without further testing or modification.

Customers are responsible for the design and operation of their applications and products using NXP Semiconductors products, and NXP Semiconductors accepts no liability for any assistance with applications or customer product design. It is customer's sole responsibility to determine whether the NXP Semiconductors product is suitable and fit for the customer's applications and products planned, as well as for the planned application and use of customer's third party customer(s). Customers should provide appropriate design and operating safeguards to minimize the risks associated with their applications and products.

NXP Semiconductors does not accept any liability related to any default, damage, costs or problem which is based on any weakness or default in the customer's applications or products, or the application or use by customer's third party customer(s). Customer is responsible for doing all necessary testing for the customer's applications and products using NXP Semiconductors products in order to avoid a default of the applications and the products or of the application or use by customer's third party customer(s). NXP does not accept any liability in this respect.

Terms and conditions of commercial sale — NXP Semiconductors products are sold subject to the general terms and conditions of commercial sale, as published at http://www.nxp.com/profile/terms, unless otherwise agreed in a valid written individual agreement. In case an individual agreement is concluded only the terms and conditions of the respective agreement shall apply. NXP Semiconductors hereby expressly objects to applying the customer's general terms and conditions with regard to the purchase of NXP Semiconductors products by customer.

Export control — This document as well as the item(s) described herein may be subject to export control regulations. Export might require a prior authorization from competent authorities.

Suitability for use in non-automotive qualified products — Unless this data sheet expressly states that this specific NXP Semiconductors product is automotive qualified, the product is not suitable for automotive use. It is neither qualified nor tested in accordance with automotive testing or application requirements. NXP Semiconductors accepts no liability for inclusion and/or use of non-automotive qualified products in automotive equipment or applications.

In the event that customer uses the product for design-in and use in automotive applications to automotive specifications and standards, customer (a) shall use the product without NXP Semiconductors' warranty of the product for such automotive applications, use and specifications, and (b) whenever customer uses the product for automotive applications beyond NXP Semiconductors' specifications such use shall be solely at customer's own risk, and (c) customer fully indemnifies NXP Semiconductors for any liability, damages or failed product claims resulting from customer design and use of the product for automotive applications beyond NXP Semiconductors' standard warranty and NXP Semiconductors' product specifications.

Translations — A non-English (translated) version of a document, including the legal information in that document, is for reference only. The English version shall prevail in case of any discrepancy between the translated and English versions.

Security — Customer understands that all NXP products may be subject to unidentified vulnerabilities or may support established security standards or specifications with known limitations. Customer is responsible for the design and operation of its applications and products throughout their lifecycles to reduce the effect of these vulnerabilities on customer's applications and products. Customer's responsibility also extends to other open and/or proprietary technologies supported by NXP products for use in customer's applications. NXP accepts no liability for any vulnerability. Customer should regularly check security updates from NXP and follow up appropriately.

Customer shall select products with security features that best meet rules, regulations, and standards of the intended application and make the ultimate design decisions regarding its products and is solely responsible for compliance with all legal, regulatory, and security related requirements concerning its products, regardless of any information or support that may be provided by NXP.

NXP has a Product Security Incident Response Team (PSIRT) (reachable at PSIRT@nxp.com) that manages the investigation, reporting, and solution release to security vulnerabilities of NXP products.

Trademarks

Notice: All referenced brands, product names, service names, and trademarks are the property of their respective owners.

NXP — wordmark and logo are trademarks of NXP B.V.

AMBA, Arm, Arm7, Arm7TDMI, Arm9, Arm11, Artisan, big.LITTLE, Cordio, CoreLink, CoreSight, Cortex, DesignStart, DynamIQ, Jazelle, Keil, Mali, Mbed, Mbed Enabled, NEON, POP, RealView, SecurCore, Socrates, Thumb, TrustZone, ULINK, ULINK2, ULINK-ME, ULINK-PLUS, ULINKpro, µVision, Versatile — are trademarks or registered trademarks of Arm Limited (or its subsidiaries) in the US and/or elsewhere. The related technology may be protected by any or all of patents, copyrights, designs and trade secrets. All rights reserved.

Airfast — is a trademark of NXP B.V.

Bluetooth — the Bluetooth wordmark and logos are registered trademarks owned by Bluetooth SIG, Inc. and any use of such marks by NXP Semiconductors is under license.

Cadence — the Cadence logo, and the other Cadence marks found at www.cadence.com/go/trademarks are trademarks or registered trademarks of Cadence Design Systems, Inc. All rights reserved worldwide.

CodeWarrior — is a trademark of NXP B.V.

ColdFire — is a trademark of NXP B.V.

ColdFire+ — is a trademark of NXP B.V.

EdgeLock — is a trademark of NXP B.V.

EdgeScale — is a trademark of NXP B.V.

EdgeVerse — is a trademark of NXP B.V.

eIQ — is a trademark of NXP B.V.

FeliCa — is a trademark of Sony Corporation.

Freescale — is a trademark of NXP B.V.

HITAG — is a trademark of NXP B.V.

ICODE and I-CODE — are trademarks of NXP B.V.

Immersiv3D — is a trademark of NXP B.V.

I2C-bus — logo is a trademark of NXP B.V.

Kinetis — is a trademark of NXP B.V.

Layerscape — is a trademark of NXP B.V.

Mantis — is a trademark of NXP B.V.

MIFARE — is a trademark of NXP B.V.

MOBILEGT — is a trademark of NXP B.V.

NTAG — is a trademark of NXP B.V.

Processor Expert — is a trademark of NXP B.V.

QorIQ — is a trademark of NXP B.V.

SafeAssure — is a trademark of NXP B.V.

SafeAssure — logo is a trademark of NXP B.V.

StarCore — is a trademark of NXP B.V.

Synopsys — Portions Copyright © 2021 Synopsys, Inc. Used with permission. All rights reserved.

Tower — is a trademark of NXP B.V.

UCODE — is a trademark of NXP B.V.

VortiQa — is a trademark of NXP B.V.

Please be aware that important notices concerning this document and the product(s) described herein, have been included in section 'Legal information'.

© NXP B.V. 2021-2022. All rights reserved.

For more information, please visit: http://www.nxp.com
For sales office addresses, please send an email to: salesaddresses@nxp.com

Date of release: 07 April 2022
Document identifier: AN13468